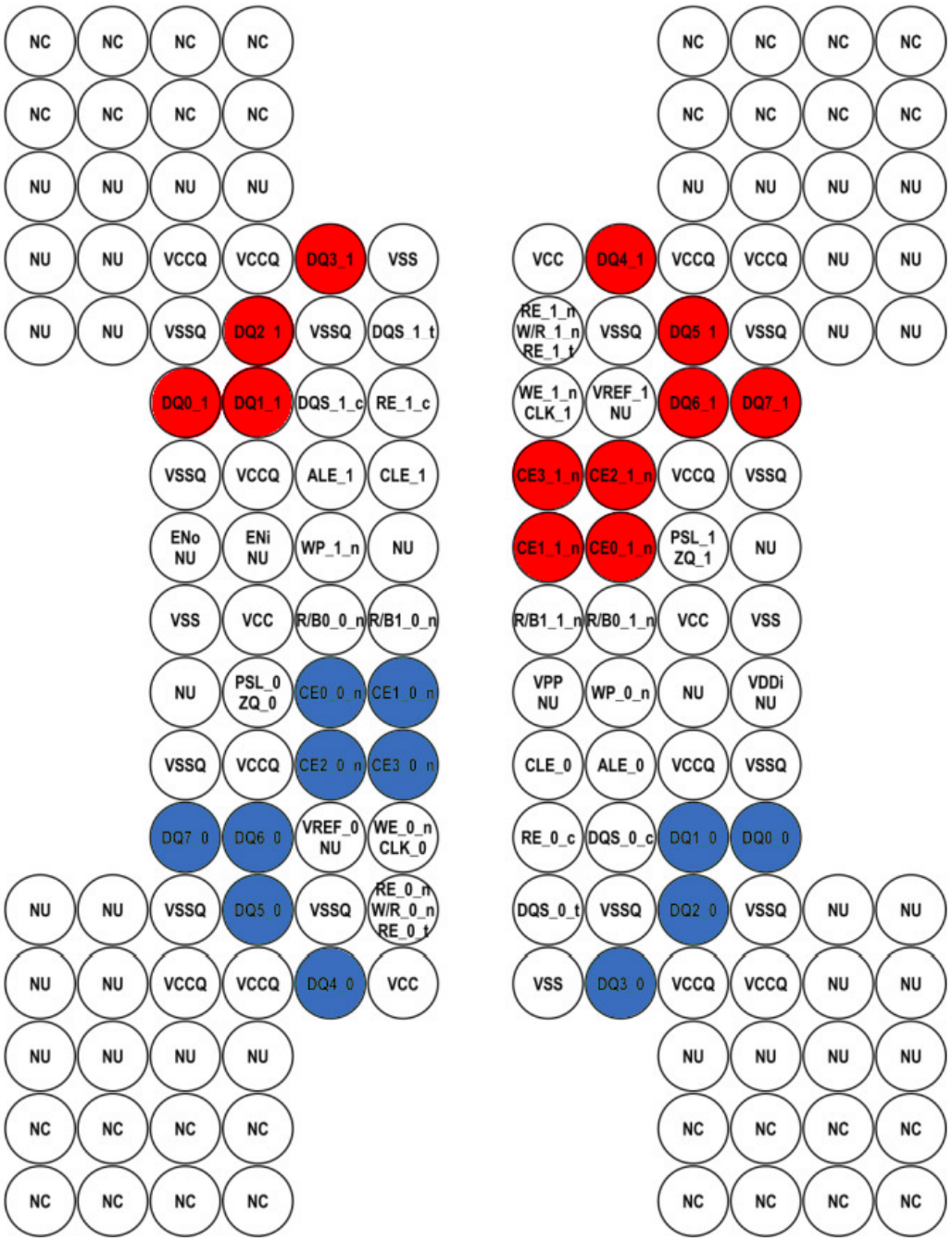
Help Center

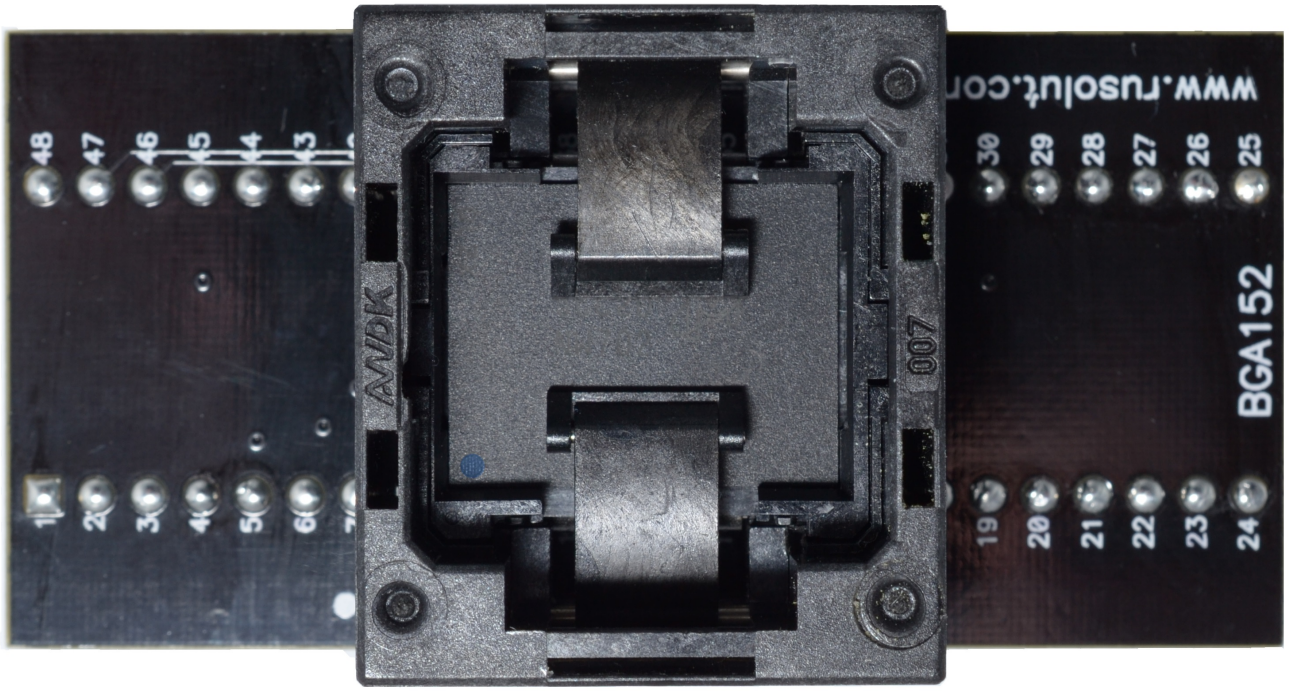
# Reading BGA132/152

High capacity BGA 132/152 chips have complex pinout which includes 2 lines of data buses and two groups of 4 CE (Crystal) signals which are connected separately to the first and the second data bus. This solution guarantees high speed of read/write operations since data can be allocated parallelly (Multi Plane Page Allocation) among crystals via each data bus. Wherefore usually those chips consist of 2 crystals, which are connected to the first and to the second data bus and it is necessary to check each group of crystals.

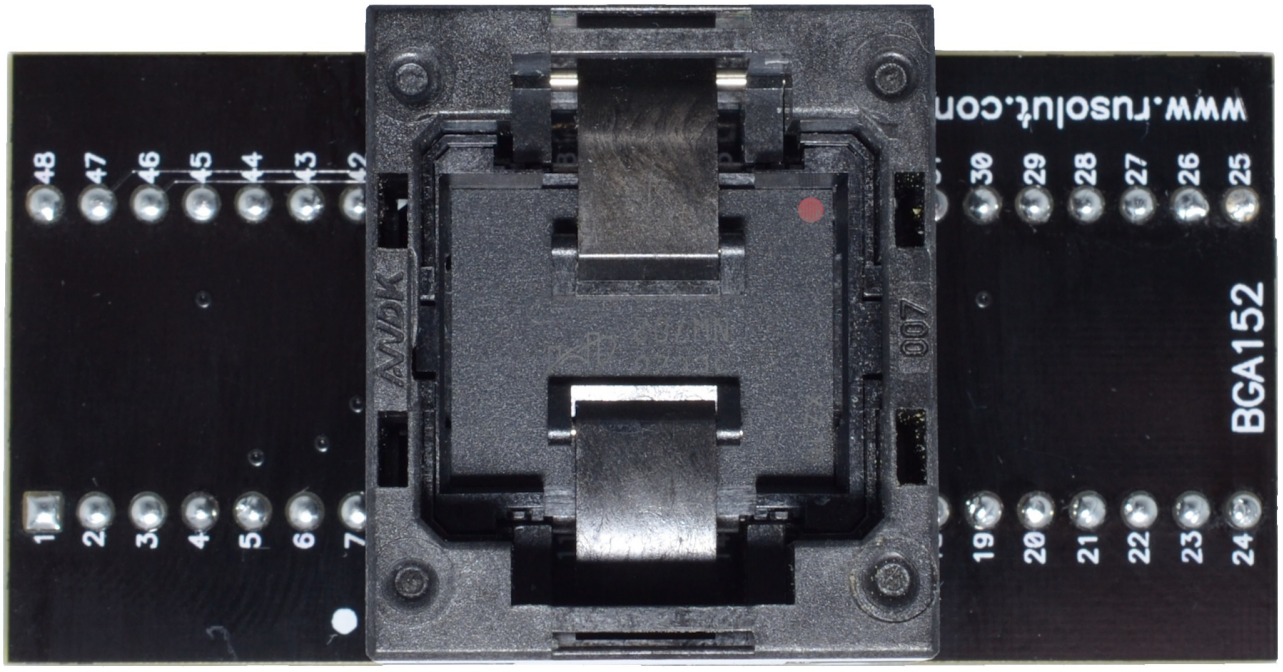
**First data bus** with its 4 CE signals is located physically on the second half of the chip and the **second data bus** is located in the first half, like on the picture below.


NC NC NC NC
NC NC NC NC
NU NU NU NU
NU NU VCCQ VCCQ DQ3_1 VSS
NU NU VSSQ DQ2_1 VSSQ DQS_1_t
DQ0_1 DQ1_1 DQS_1_c RE_1_c
VSSQ VCCQ ALE_1 CLE_1
ENo NU ENi NU WP_1_n NU
VSS VCC R/B0_0_n R/B1_0_n
NU PSL_0 ZQ_0 CE0_0_n CE1_0_n
VSSQ VCCQ CE2_0_n CE3_0_n
DQ7_0 DQ6_0 VREF_0 NU WE_0_n CLK_0
NU NU VSSQ DQ5_0 VSSQ RE_0_n W/R_0_n RE_0_t
NU NU VCCQ VCCQ DQ4_0 VCC
NU NU NU NU
NC NC NC NC
NC NC NC NC
NC NC NC NC
NC NC NC NC
NU NU NU NU
VCC DQ4_1 VCCQ VCCQ NU NU
RE_1_n W/R_1_n RE_1_t VSSQ DQ5_1 VSSQ NU NU
WE_1_n CLK_1 VREF_1 NU DQ6_1 DQ7_1
CE3_1_n CE2_1_n VCCQ VSSQ
CE1_1_n CE0_1_n PSL_1 ZQ_1 NU
R/B1_1_n R/B0_1_n VCC VSS
VPP NU WP_0_n NU VDDi NU
CLE_0 ALE_0 VCCQ VSSQ
RE_0_c DQS_0_c DQ1_0 DQ0_0
DQS_0_t VSSQ DQ2_0 VSSQ NU NU
VSS DQ3_0 VCCQ VCCQ NU NU
NU NU NU NU
NC NC NC NC
NC NC NC NC

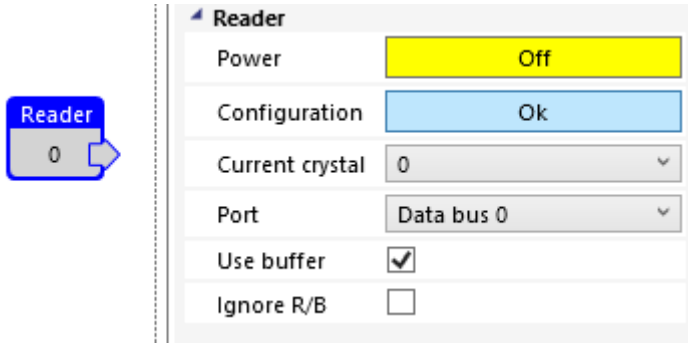
Dumps from the **first group** of crystals can be read while chip is placed in default orientation in the adapter.

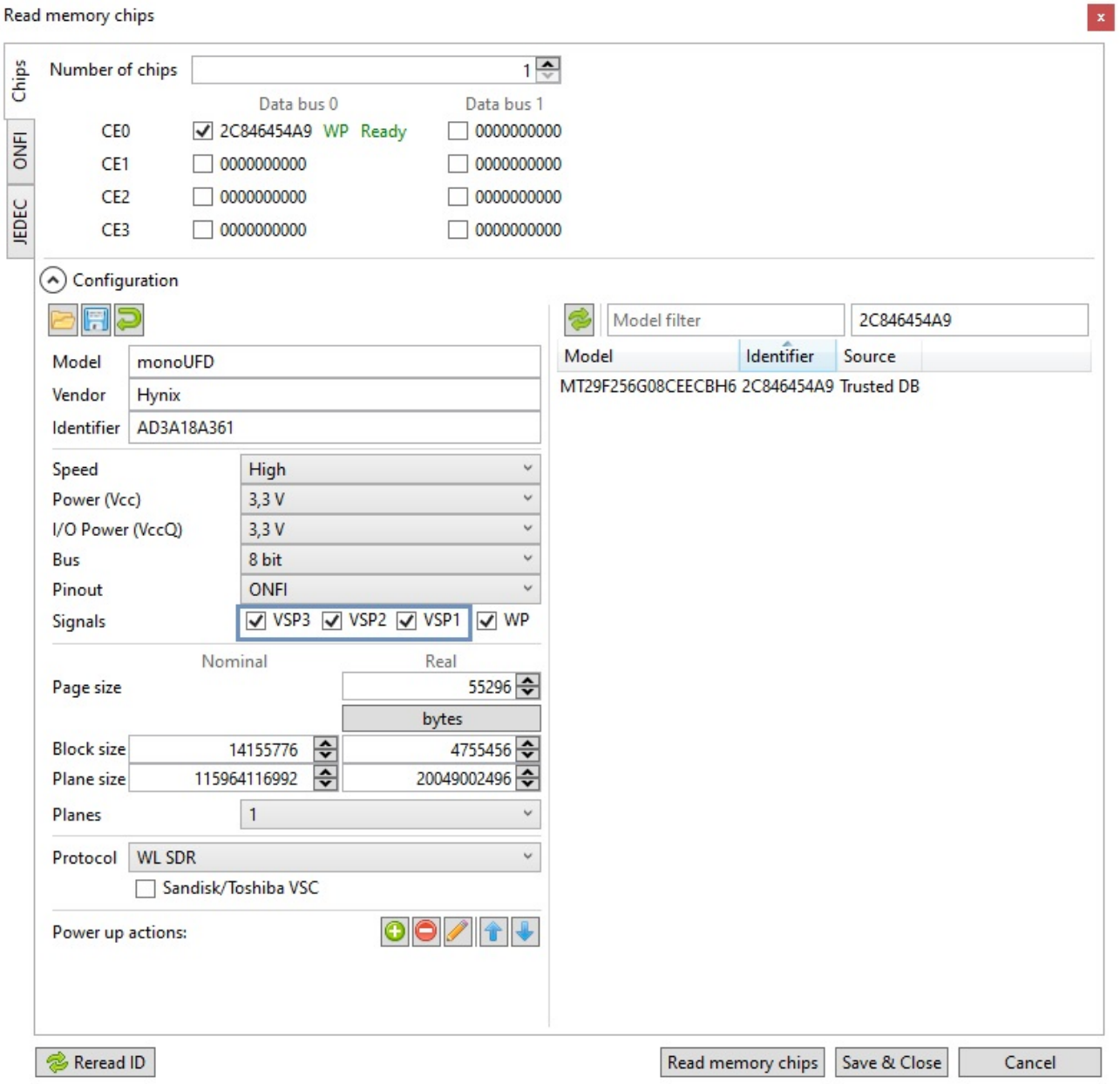



In order to read the dumps from the **second group,** it is necessary to put the chip in reversed orientation inside the adapter

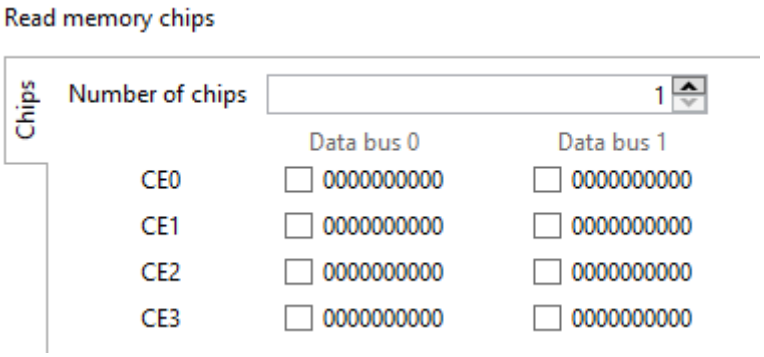



and switch VSP1,2,3 checkboxes in the reader configuration menu.




If the chip doesn't have connected crystals to the **second data bus** VNR will not display ID.

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